

S/N 09/945,500PATENTIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes  
Serial No.: 09/945,500  
Filed: August 30, 2001  
Title: PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH  
LOW TUNNEL BARRIER INTERPOLY INSULATORS

Examiner: Ly D. Pham  
Group Art Unit: 2827  
Docket: 1303.029US1

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Mail Stop 313 (c)  
Commissioner for Patents  
Office of Petitions  
Madison West Building, 7th Floor  
600 Dulany Street  
Alexandria, VA 22313

FAX RECEIVED

JUL 11 2005

OFFICE OF PETITIONS

Applicant would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date/Issue Date</u>	<u>Attorney Docket</u>	<u>Title</u>
11/062543	February 22, 2005	1303.028US2	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
11/063825	February 23, 2005	1303.132US1	GERMANIUM-SILICON-CARBIDE FLOATING GATES IN MEMORIES

Continuations and divisionals may be later filed on the cases listed above, or cited to the Examiner in any previous Communication Concerning Related Applications. Applicants request that the Examiner review all continuations and divisionals of the above-listed or previously-cited patent applications before allowing the claims of the present patent application.

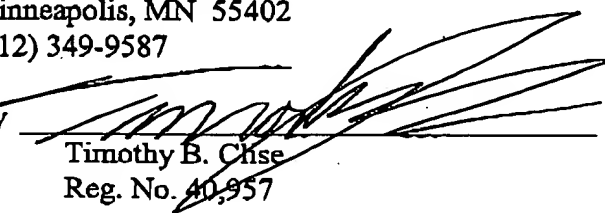
Respectfully submitted,  
LEONARD FORBES

By Applicant's Representatives,  
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
P.O. Box 2938  
Minneapolis, MN 55402  
(612) 349-9587

Date

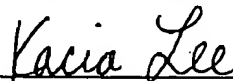
11 July '05

By

  
Timothy B. Chase  
Reg. No. 40,957

I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

Kacia Lee



Date of Transmission

July 11, 2005